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10/715,741	11/18/2003	Kenji Kimura	P8414a	4383

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EXAMINER	
DANIELS, ANTHONY J	
ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,741	KIMURA ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-7,9,11,12 and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (US # 4,910,599).

As to claim **1**, Hashimoto teaches an image sensor controller (Figure 9, driver "206") for controlling an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller (Figure 10, clock "207") configured to supply to the transfer section, which shifts and transfers received image data, a shift/transfer clock for shifting and transferring the image data (Col. 12, Lines 34-36), wherein the light receiving section comprises a dummy pixel region (Figure 9, optical black portion "OB") and an effective pixel region (Figure 9, effective portion "B"), and wherein the shift/transfer clock supplied by the drive controller to the transfer section has a clock frequency that is higher in a dummy pixel output period during which image data obtained from the dummy

pixel region is outputted from the transfer section than in an effective pixel output period during which image data obtained from the effective pixel region is outputted from the transfer section (Figure 11A, pulses more frequent in T_{VOB} than in T_{VB}; Col. 13, Lines 4-20).

As to claim **2**, Hashimoto teaches an image sensor controller (Figure 9, driver "206") for controlling an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller (Figure 10, clock "207") configured to supply to the transfer section, which shifts and transfers received image data, a shift/transfer clock for shifting and transferring the image data (Col. 12, Lines 34-36), wherein a reading pixel region in which image data is read (Figure 9, effective portion "B") and a non-reading pixel region in which image data is not read are defined (Figure 9, unnecessary portions "A" and "C"), and wherein the shift/transfer clock supplied by the drive controller to the transfer section has a clock frequency that is higher in a non-reading pixel output period during which image data obtained from the non-reading pixel region is outputted from the transfer section than in a reading pixel output period during which image data obtained from the reading pixel region is outputted from the transfer section (Figure 11A, pulses more frequent in T_{VA} and T_{VC} than in T_{VB}; Col. 13, Lines 4-20).

As to claim **3**, Hashimoto teaches an image sensor controller (Figure 9, driver "206") for controlling an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller (Figure 10, clock "207") configured to supply to the transfer section, which shifts and transfers received

image data, a shift/transfer clock for shifting and transferring the image data (Col. 12, Lines 34-36), wherein a reading pixel region in which image data is read (Figure 9, effective portion "B"), a non-reading pixel region in which image data is not read (Figure 9, unnecessary portions "A" and "C"), and a dummy pixel region are defined (Figure 9, optical black portion "OB"), and wherein the shift/transfer clock supplied by the drive controller to the transfer section has a clock frequency that is highest in a dummy pixel output period during which image data obtained from the dummy pixel region is outputted from the transfer section, next highest in a non-reading pixel output period during which image data obtained from the non-reading pixel region is outputted from the transfer section, and lowest in a reading pixel output period during which image data obtained from the reading pixel region is outputted from the transfer section (Figure 11A).

Remarks about claim 3: The language "highest", "next highest" and "lowest" does not clearly state of which clock pulses the specific pulse frequency is the highest, next highest or lowest. The pulse for the optical black (dummy) portion has the highest frequency of the optical black portion frequency and the effective (reading) portion frequency. The pulse for the unnecessary (non-reading) portion has the next highest frequency when compared with the effective portion frequency. The effective portion frequency is the lowest of three frequencies.

As to claim **4**, Hashimoto teaches an image sensor controller according to claim 1, wherein the drive controller includes a pattern selector configured to select, from among a plurality of clock patterns for setting the shift/transfer clock, a specific clock pattern for each period during which image data is outputted from the transfer section of the image sensor (Figure 11A).

As to claim **5**, the limitations of claim 5 can be found in claim 4. Therefore, claim 5 is analyzed and rejected as previously discussed with respect to claim 4.

As to claim **6**, the limitations of claim 6 can be found in claim 4. Therefore, claim 6 is analyzed and rejected as previously discussed with respect to claim 4.

As to claim **7**, Hashimoto teaches an image sensor controller according to claim 4, wherein the drive controller includes a memory configured to store the plurality of clock patterns (*It is inherent in the embodiment that there is a memory for storing instructions for setting the clock patterns of Figure 11A.*), and the pattern selector selects from among the plurality of clock patterns stored in the memory a specific clock pattern for each image data output period based on pattern switch timing setting information, and supplies the shift/transfer clock to the transfer section of the image sensor based on the clock pattern selected (Figure 11A).

As to claim **9**, Hashimoto teaches an image sensor controller according to claim 3, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog image data sent from the transfer section of the image sensor to digital image data and (ii) receive the digital image data outputted from the A/D converter based on the supplied A/D conversion/transfer clock, wherein the image processing controller disables an output operation of the A/D converter during periods in which the A/D converter outputs image data obtained from the dummy pixel region and non-reading pixel region (*Neither the unnecessary pixel data nor the optical black pixel data is output by the A/D converter inherent in the device of Hashimoto. Thus, the output of the A/D converter is disabled from outputting the unnecessary data and the optical black data.*).

As to claim **11**, Hashimoto teaches image sensor controller (Figure 9, driver "206") for controlling an image sensor (Figure 9 and 10, CCD "201"; Col. 12, Lines 32-36) having a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19), the image sensor controller comprising: a drive controller (Figure 10, clock "207") configured to supply to the transfer section, which shifts and transfers received image data, a shift/transfer clock for shifting and transferring the image data (Col. 12, Lines 34-36), the drive controller including a pattern selector configured to select, from among a plurality of clock patterns for setting the shift/transfer clock, a specific clock pattern for each period during which image data is outputted from the transfer section of the image sensor, and wherein the frequency of the shift/transfer clock supplied during a particular period is based on the specific clock pattern selected for that period (Figure 11A).

As to claim **12**, Hashimoto teaches an electronic device (Figure 10), comprising: an image sensor (Figure 10, CCD "201") that has a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19); an image sensor controller (Figure 10, driver "206") configured to control the image sensor (Col. 12, Lines 33-36), the image sensor controller comprising a drive controller configured to supply to the transfer section, which shifts and transfers received image data, a shift/transfer clock for shifting and transferring the image data (Col. 12, Lines 33-36), wherein the shift/transfer clock supplied by the drive controller to the transfer section has a frequency that is higher in a dummy pixel output period during which image data obtained from a dummy pixel region (Figure 9, "OB") is outputted from the transfer section than in an effective pixel output period during which image

data obtained from an effective pixel region (Figure 9, "B") is outputted from the transfer section (Figure 11A, pulses more frequent in TVOB than in TVB; Col. 13, Lines 4-20).

As to claims **14,15,17** and **18**, claims 14,15,17 and 18 are method claims corresponding to the apparatus claims 1,2,4 and 5, respectively. Therefore, the method claims 14,15,17 and 18 are analyzed and rejected as previously discussed with respect to apparatus claims 1,2,4 and 5, respectively.

As to claim **16**, Hashimoto teaches a method for controlling an image sensor (Figure 10, CCD "201") having a light receiving section and a transfer section that receives image data from the light receiving section (Col. 12, Lines 15-19), the method comprising: controlling the frequency of a shift/transfer clock for shifting and transferring image data by setting the frequency of the shift/transfer clock to a first frequency in a dummy pixel output period during which image data obtained from a dummy pixel region is outputted from the transfer section (Figure 11A, TVOB; Col. 13, Lines 4-20), setting the frequency of the shift/transfer clock to a second frequency in a non-reading pixel output period during which image data obtained from a non-reading pixel region is outputted from the transfer section (Figure 11A, TVA and TVC; Col. 13, Lines 4-20), and setting the frequency of the shift/transfer clock to a third frequency in a reading pixel output period during which image data obtained from a reading pixel region is outputted from the transfer section (Figure 11A, TVB; Col. 13, Lines 4-20); and supplying the shift/transfer clock to the transfer section which shifts and transfers received image data based on the frequency of the shift/transfer clock (Col. 12, Lines 33-36).

As to claim **19**, the limitations of claim 19 can be found in claim 17. Therefore, claim 19 is analyzed and rejected as previously discussed with respect to claim 17.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Hata (US # 6,100,928).

As to claim **8**, Hashimoto teaches an image sensor controller according to claim 3, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog image data sent from the transfer section of the image sensor to digital image data and (ii) receive the digital image data outputted from the A/D converter based on the supplied A/D conversion/transfer clock (*A/D conversion circuits are inherent in CCD imaging applications.*), wherein the image processing controller invalidates image data obtained from dummy pixel region (*Dummy pixel data is not included in the effective*

imaging. Therefore, it is invalidated as image data at some point.) and the non-reading pixel region (Col. 13, Lines 33-58). The claim differs from Hashimoto in that it further requires that the image processing controller invalidates image data received from A/D converter.

In the same field of endeavor, Hata teaches a digital camera comprising a CCD which outputs image data to an A/D converter before it is input to an image processing device (Figure 1, A/D "106", IPP "107"). In light of the teaching of Hata, it would have been obvious to one of ordinary skill in the art to include the A/D converter before image processing in the system of Hata, because an artisan of ordinary skill in the art would recognize the numerous advantages of digital processing over analog processing.

2. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Kochi (US # 5,191,426).

As to claim **10**, Hashimoto teaches an image sensor controller according to claim 1, further comprising: an image processing controller configured to (i) supply an A/D conversion/transfer clock to an A/D converter that converts analog image data sent from the transfer section of the image sensor to digital image data and (ii) receive the digital image data outputted from the A/D converter based on the supplied A/D conversion/transfer clock (*A/D conversion circuits are inherent in CCD imaging applications.*). The claim differs from Hashimoto in that it further requires that the image processing controller supplies the A/D conversion/transfer clock at a constant clock frequency, irrespective of the changes in frequency of the shift/transfer clock.

In the same field of endeavor, Kochi teaches a CCD image pickup device including an A/D converter clocked at a constant timing frequency (Col. 5, Lines 3-7). In light of the teaching of Kochi, it would have been obvious to include a constant timing clock frequency for the A/D converter in Hashimoto, because an artisan of ordinary skill in the art would recognize that this clock could also function as the timing for the effective region of the CCD in Hashimoto (see Kochi, Col. 5, Lines 3-7).

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US # 4,910,599) in view of Potucek et al. (US # 5,684,609).

As to claim **13**, Hashimoto teaches an electronic device according to claim 12. The claim differs from Hashimoto in that it further requires a carriage on which the image sensor is mounted; a drive device configured to drive the carriage in a scanning direction; a servo controller configured to perform servo control on the drive device in accordance with servo control information read by the image sensor from a source.

In the same field of endeavor, Potucek et al. teaches an image scanner which reads effective imaging pixels and dark pixels for FPN reduction (Figure 1; Col. 3, Lines 15-44). In light of the teaching of Potucek et al., it would have been obvious to one of ordinary skill in the art to include the increased image output method in the scanner of Potucek et al., because an artisan of ordinary skill in the art would recognize that this would lead to increased scan rates for the image scanner of Potucek et al. (see Hashimoto, Col. 2, Lines 29-35).

The examiner takes **Official Notice** that image scanners complete with a carriage, drive device and servo control are well known and expected in the art. One of ordinary skill in the art

would recognize that these components allow for effective and precise operation of an image scanner.

Conclusion

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
5/22/2007

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